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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,926	03/25/2004	Yu Jen Chen	24061.103 (TSMC2003-0449)	1917

42717 7590 07/24/2007

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
07/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,926	CHEN ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-15 and 19-22* is/are rejected.

7)☒ Claim(s) *16-18* is/are objected to.

8)☒ Claim(s) *23-26* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/810,926 and response filed on 5/29/2007. Claims 13-26 remain pending in the application, where claims 1-12 are canceled and claims 23-26 are newly added.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 13-15 and 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Torres et al. "The Virtual Fab the Core of Future Technology Development", IEEE, 1999, pages 222-226.

4. As to claim 13, Torres et al. the Vitual Fab that is the core of future technology development. The virtual fab comprising a web tracking system for semiconductor manufacturing processing (see whole documents). The virtual fab allows design information (transistor data or other semiconductor device data to be processed and manufactured) to be shared and tracked by partners. A semiconductor manufacture produces a semiconductor device for customers. The partners described herein are interpreted as including a manufacturer, customers and other entities involved in the manufacturing process. The design information shared and tracked by partners must include changes in the design information (transistor data for their new films, processes and new materials) that impact the manufacture of a semiconductor device (transistors)

fro the customer. The design database is inherently within the art and used to store design related information and shared by different entities. This is due to the web tracking system. The web tracking system as taught by Torres would shorten the cycle time of bringing innovation between entities and enable suppliers to develop equipment/material for advanced processing in the shortened time possible.

5. As to claim 14, Torres et al. teach an innovation of web tracking system that can be used to interactively shared design information between entities. A manufacturer of semiconductor device produces a semiconductor product for customers. The web tracking system as taught by Torres et al. would allow a customer to access design information from the design database to design a semiconductor device because the web tracking system (Internet) is known to be used for quickly accessing information including design related information.

6. As to clam 15, Torres et al. teach an innovation of web tracking system that can be used to interactively tracked and shared design information between entities. The web tracking system must include a design coordination engine that is used to interactively tracked and shared semiconductor design related information. The web tracking system must include time stamps that record login and logout because this is part of normal process of Internet. Therefore the web tracking system would also allow record time stamps of customer who access the design database.

7. As to claim 19, Torres et al. teach an innovation of web tracking system operated through the World Wide Web (page 223). The Virtual Fab that includes a web tracking system closely links all entities together where resources (semiconductor design related

information) can be shared and access by all entities as needed (see whole document). The paper as taught by Torres et al. will highlight how the virtual fab can reduce the cost, time and risk of research and development and assist universities in transforming their ideas into manufacturable solution. Suppliers with new materials will be able to test them out on SEMATECH's latest process. When a transistor lot is ordered by a supplier, university or member company, SEMATECH will process the lot and sent it to other facilities (notifying other entities) to add process steps that are not available at SEMATECH. In this way, the web tracking system closely links all entities together by sending information/notifying/alerting through the World Wide Web. From these teachings, the web tracking system operated through a World Wide Web as taught by Torres et al. must include a design coordination engine including an appraisal module in order to evaluate costs related to manufacturing of semiconductor device.

8. As to claims 20-22, Torres et al. teach a web tracking system operated through a World Wide Web, where resources (design information) related to semiconductor manufacturing can be shared/tracked/notified by and to entities (whole document). The design database is used to stored related design information of semiconductor device. Since the sub-databases are known to practitioners and they can be created as needed, the limitation of design database that includes an associated building block sub-database for technology and a customer design profile is inherently included because they can be created for storing related design information, technology and customer profile as needed.

Allowable Subject Matter

9. Claims 23-26 are allowed over the prior art of record.

10. Claims 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest all claims limitations as recited in the claims.

Remarks

11. Applicants remarks have reviewed and not persuasive. Applicants argued that Torres fails to teach tracking changes in the design change information that impact the manufacturing of a semiconductor device for the customer. Torres teaches the virtual Fab for the Core of Future Technology Development including a web tracking system (see page 222). The Virtual Fab includes SEMANTECH's Front End Processes (FEP) projects that involve partnerships among universities, equipment/material suppliers, member companies and SEMANTECH named different entities. The partnerships between different entities including SEMANTECH's Front End processes in manufacturing of a semiconductor device resolves complex solutions because the Virtual Fab allows partners to share transistor processing across (design information) multiple entities or sites. Torres teaches the invention to manufacturing of a semiconductor device. The Virtual Fab includes SEMANTECH's front end processes of manufacturing of a semiconductor device. Examiner respectively submits the manufacturing embraces a design process, a mask fabrication process and a

semiconductor fabrication process. Because Torres teaches that the SEMANTECH's FEP allows partners (designers) to share transistor processing across multiple entities (laboratories, manufacturing) and the Virtual Fab includes a web tracking system, Examiner believes that the web tracking system is used for tracking changes in design information that impact the manufacturing of a semiconductor device for the customer. Examiner disagrees with Applicants that Torres only teaches tracking wafer's locations. It is not true. Torres teaches as the wafers travel through the Virtual Fab, the plan is to give users (designers) the capability to track wafers and access final electrical test data through the World Wide Web (page 223). Tracking the wafers here mean tracking changes in the design information (circuit data such as transistor, gate dielectric, gate electrodes, ultra-shallow junctions and others to manufacturing). The wafer includes mask data of layout pattern that needed to be tested during the design process (Front End processes). Before fabrication, the wafer including mask data of layout pattern need to be tested and the design information (circuit data) needed to be changed to make any necessary improvement. The tracking system that includes in the Virtual Fab would track and record all these changes of the design information that impact the manufacturing of a semiconductor device for the customer. Therefore the teachings of Torres as described in the article anticipated the overly broad claim 13.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, A.U. 2825